**In the Specification**

Please amend the specification as follows (A marked up version of the amended specification is attached):

Page 2, Paragraph beginning at line 3:

A1 The present invention relates to a liquid crystal display, and more particularly, to a TFT (Thin Film Transistor) LCD (Liquid Crystal Display) having a large aperture ratio.

Page 2, Paragraph beginning at line 6:

Referring to FIG. 1A, an AMLCD (Active Matrix Liquid Crystal Display Device) used in a portable TV or a notebook computer, or the like is provided with a plurality of scanning lines 10 and signal lines 17 crossing each other, and pixel regions defined by the scanning lines 10 and the signal lines 17. These are TFTs at parts where the scanning lines 10 and the signal lines are A2 crossed; and pixel electrodes (dashed lines in the drawing) in the pixel regions for displaying a desired picture when a voltage is applied to the scanning lines 10, to switch the TFT, and to transmit a picture signal provided to the signal lines 17 to the pixel electrodes.

[Page 2, Paragraph beginning at line 13:]

Referring to FIG. 1B showing a section across line A-A', the AMLCD is provided with a gate electrode 11 on a transparent substrate 7, and a gate insulating layer 13 on the gate electrode 11. There is a channel layer 15 and an ohmic contact layer 16 of amorphous silicon a-Si on the gate insulating layer 13, and source/drain electrodes 17a and 17b on the ohmic contact layer 16. There is a protection layer 19 on an entire surface of the source/drain electrodes 17a and 17b, a contact hole 20 in the protection layer 19. The pixel electrode 21 and the drain electrode 17b are connected through the contact hole 20. In the drawing, Cgs denotes a capacitance between the gate electrode and the source electrode, Cgd denotes a capacitance between the gate electrode and the drain electrode. The Ccross denotes a capacitance in overlap regions of the scanning lines and the signal lines. The Cgs, Cgd, and Ccross are parameters influencing to an accumulated capacitance (not shown), as well as $\Delta$ Vp (change in offset voltage) and $\Delta$ Vpxl (change in pixel voltage). In the related art LCD, if there is a misalignment between the

scanning line 10 and the signal line 17, minute variations of Cds and Cgd give influence to Δ Vp and Δ Vpxl, making flicker worse and causing non-uniform luminance, that deteriorates a picture quality. And, in a divided exposure for a large sized screen, the increased deviations of Cgs and Cgd caused by poor adjustment between shots worsens the foregoing problem, to impede providing a large sized LCD screen, and, since the TFT is formed on an extension line of the scanning line, to reduce an aperture ratio of the device.

A2

Page 3, Paragraph beginning at line 15:

A3

Another object of the present invention is to provide TFT LCD which shows no deterioration of a picture quality even in divided exposure for a large sized screen.

Page 5, Paragraph beginning at line 12:

A4

Referring to FIG. 2B, the LCD in accordance with a preferred embodiment of the present invention includes a scanning line (a gate electrode) 111 of a metal, such as aluminum, formed on a transparent substrate 107 by sputtering. There is an insulating layer 113 of SiNx or SiOx or the like formed thereon by APCVD (Atmospheric Chemical Vapor Deposition), and a semiconductor layer 115 and an n+ layer 115 stacked in succession thereon. The semiconductor layer 115 is formed of amorphous silicon a-Si, and the insulating layer 113 is formed of $SiO_2$ having good bulk characteristics, and can prevent short circuit of the gate electrode 111 and formation of hillock at the gate electrode 11 without an anodized film. There are a channel layer and an ohmic contact layer formed by etching the semiconductor layer 115 and the n+ layer 116, and source/drain electrodes 117a and 117b of aluminum or chromium formed by sputtering and patterning. The ohmic contact layer 116 is formed by dry etching by using the source/drain electrode 117a and 117b as a mask. There is a protection layer 119 of SiNx on an entire surface of the substrate 107 formed by PECVD (Plasma Enhanced Chemical Vapor Deposition), and a pixel electrode 121 thereon in a pixel region formed by sputtering and patterning ITO (Indium Tin Oxide). The pixel electrode 121 is connected to the drain electrode 117b electrically through a contact hole 120 in the protection layer 119. The channel layer 115 has a width smaller than the widths of the scanning line 111 and the signal line 117a, and is positioned between the scanning line 111 and the signal line 117a. In this instance, since the channel layer 115 is covered with the signal line 117a, generation of off-current is prevented, to prevent deterioration